CS23402 COMPUTER ARCHITECTURE

1. Design a hardware to support out of order execution with speculation. (5)

2. Consider the code example for Tomasulo's algorithm with speculation: (5)

   ```
   fld f0,0(x1)
   fmul.d f4,f0,f2
   fsd f4,0(x1)
   addi x1,x1,_8
   ```

   Assume that we have issued all the instructions. Let's also assume that the fld and fmul.d have committed and all other instructions have completed execution. Fill all the information tables.

3. Explain 2 bit branch predictor? What if we increase bits? Compute size required with 1k entries and bits in address.